REMARKS

Applicants appreciate the Examiner's attention to this application. This response cancels claims 1, 7, 16, 25, 28, 31-46, and 52. This response adds claims 61-75. This response amends claims 2-6, 8-15, 17-24, 26-27, 29-30, 47-51, and 53-60.

Claims 61, 62, 74, and 75 are the pending independent claims. Reconsideration of the present application in view of the enclosed amendments and remarks is respectfully requested.

ARGUMENT

The Office Action includes rejections based on 35 U.S.C. §§ 112 (second paragraph), 101, 102(e), and 103(a). To the extent that any of those rejections might be applied to the claims as amended, Applicants respectfully traverse.

35 U.S.C. § 112, Second Paragraph

The Office Action rejects claims 3-15, 18-30, 33-45, and 48-60 under 35 U.S.C. § 112, second paragraph, because of insufficient antecedent basis for the term "the identifiers" in claims 3, 18, 33, and 48. The claim amendments in this response overcome this rejection.

35 U.S.C. § 101

The Office Action provisionally rejects claims 1, 16, 31, and 46 under 35 U.S.C. § 101, on the basis of statutory double patenting, in light of U.S. patent application no. 09/540,613 (attorney docket no. P8628). This response cancels claims 1, 16, 31, and 46 and adds new independent claims that do not match any of the claims in U.S. patent application no. 09/540,613.

35 U.S.C. § 102(e)

The Office Action rejects claims 1, 16, 31, and 46 under 35 U.S.C. § 102(e) as being anticipated by U.S. patent no. 6,292,874 to Philip C. Barnett (hereinafter "Barnett"). To the extent those rejections might be applied to the claims of the present application, as amended, Applicants respectfully traverse.

Embodiments of the present invention relate to a processing system with one or more processors, a chipset circuit, and a processor nub loader for loading processor nub that provides the initial set-up and low-level management of isolated memory in the processing system. The processor nub and the processor nub loader may also be referred to as a processor executive (PE) and a PE handler, respectively. (See, e.g., Detailed Description page 12, line 6, through page 14, line 6.)

Claim 61 in the present application recites an apparatus comprising (a) a processor that can operate in normal execution mode and in "isolated execution mode," (b) memory to include an "isolated memory area accessible to the processor in the isolated execution mode," and (c) storage to store a "PE handler image" to be loaded into the "isolated memory area." The other pending independent claims (i.e., claims 62, 74, and 75) involve features that are the same as or similar to the features quoted above with regard to claim 61.

By contrast, Barnett relates to a "memory management circuit for a single chip processing circuit, such as a smart card" (col. 2, lines 47-65). Accordingly, Barnett discusses memory management and security in the context of a single chip processing circuit. Unlike the present application, Barnett says nothing about chipset circuits, processor nubs, or PE handlers.

In the present application, claim 61 not only involves a chipset circuit and a PE handler image, but also includes language describing a source and a destination for a PE handler image. Barnett clearly does not anticipate an apparatus with storage to store a "PE handler image" to be loaded into an "isolated memory area."

Accordingly, Barnett does not anticipate any of the pending independent claims.

35 U.S.C. § 103(a)

The Office Action rejects claims 2, 17, 32, and 47 under 35 U.S.C. § 103(a) as being unpatentable over Barnett in view of U.S. patent no. 6,035,374 to Ramesh Panwar et al. (hereinafter "Panwar"). To the extent those rejections might be applied to the claims of the present application, as amended, Applicants respectfully traverse.

Panwar relates to a method for "dynamically reconfiguring a processor between uniprocessor and selected multiprocessor configurations" (col. 2, lines 43-48). Neither Panwar nor Barnett provides a motivation to combine Panwar and Barnett.

Additionally, even if Barnett and Panwar were to be combined, the combination would not disclose or suggest all of the features recited in claim 2. For instance, claim 2 involves a thread count indicating the "number of threads currently initialized for operation in the isolated execution mode." Neither Barnett nor Panwar disclose the concept of maintaining a count of threads currently operating in a particular mode. Consequently, a combination of Barnett and Panwar would not teach the concept of maintaining a count of the number of threads currently operating in the isolated execution mode.

In addition, references cannot render a dependent claim obvious unless they also disclose or suggest the features of the corresponding independent claim. Barnett and Panwar, however, even if combined, do not teach the features discussed above with regard to the § 102(e) rejections of the independent claims. Claim 2, for instance, depends from, and therefore implicitly includes the features of, claim 74. However, like Barnett, Panwar does not disclose or suggest a PE handler image to be loaded into an isolated memory area of a processing system.

Also, claims 17, 47, and 63 involve features that are the same as or similar to those discussed above with regard to claim 2. Consequently, claims 2, 17, 47, and 63, patentably define the invention over the cited art.

The Office Action rejects claims 3-14, 18-29, 33-44, and 48-59 under 35 U.S.C. § 103(a) as being unpatentable over Barnett and Panwar and further in view of U.S. patent application publication no. 2002/0007456 A1 to Marcus Peinado et al.

(hereinafter "Peinado"). Also, the Office Action rejects claims 15, 30, 45, and 60 under 35 U.S.C. § 103(a) as being unpatentable over Barnett, Panwar, and Peinado, and further in view of U.S. patent no. 6,507,904 to Carl M. Ellison et al. (hereinafter "Ellison"). To the extent those rejections might be applied to the claims of the present application, as amended, Applicants respectfully traverse.

The present application has a filing date of September 22, 2000, and also claims priority to an application with a filing date of March 31, 2000. The filing date of Peinado, however, is June 27, 2001. Since Peinado does not predate the present application, Peinado does not qualify as prior art.

For reasons including those set forth above, the Office Action fails to make out a *prima facie* case of obviousness for any of the pending claims. In addition, the pending claims recite numerous additional features that are not disclosed or suggested by any of the cited art.

For these and other reasons, all pending claims are allowable.

INFORMATION DISCLOSURE STATEMENT

The Office Action included copies of all information disclosure statements (IDSs) submitted as of April 7, 2004, with initials from the Examiner for most references. However, those copies did not include initials from the Examiner for one of the five references listed on page one of the IDS submitted on November 18, 2002. Applicants respectfully request confirmation that the Examiner has considered all references listed on that IDS.

CONCLUSION

In view of the foregoing remarks, claims 2-6, 8-15, 17-24, 26-27, 29-30, 47-51, and 53-75 are all in condition for allowance.

As indicated above, Applicants also request confirmation that all references cited by Applicants have been considered.

If the Examiner has any questions, the Examiner is invited to contact the undersigned at (512) 732-3927. Early issuance of Notice of Allowance is respectfully requested.

Respectfully submitted,

Dated: 6/17/04

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